C8051F120 UARTn Configuration (read Technical Summary, Ch. 21 & 22 for details; n = 0 or 1)

1. Serial Control Register – SCON0 (0x98, Page 0) & SCON1 (0x98, Page 1)
   SM0n, SM1n: Mode – 8/9 bits, Synchronous/Asynchronous
   SM2n: Valid Stop Bit checking
   RENn: Enable Receiver (turn off to save power and disable incoming characters)
   TB8n: TX Data for 9th bit (MSB after [7-0] in data register)
   RB8n: RX Data for 9th bit (MSB after [7-0] in data register)
   TIn: Flag set on Transmit Complete, generates Interrupt if Interrupt is enabled
   RIn: Flag set on Receive Complete, generates Interrupt if Interrupt is enabled
      NOTE: a single interrupt vector is shared between transmit & receive, but the flags are separate
      UART0 uses Interrupt Priority 1
      UART1 uses Interrupt Priority 20

2. Serial Status Register – SSTA0 (0x91, Page 0)
      There is no SSTA1; UART1 has fewer operating options
   FE0: Frame Error Flag (invalid STOP bit detected – usually a problem caused by the transmitter)
   RXOV0: Receiver Overrun Flag (new data has arrived before previous byte was read)
   TXCOL0: Transmission Collision Flag (new data stored in buffer before previous byte transmission complete)
      FE, RXOV, & TXCO are the only 3 possible error conditions allowed
   SMOD0: Baud Rate Doubler Enabler (enables or disables divide-by-2 logic)
   S0TCLK1, S0TCLK0: Transmit Clock Source (for Baud Rate)
   S0RCLK1, S0RCLK0: Receive Clock Source (for Baud Rate)

3. UARTn Data Buffer – SBUF0 (0x99, Page 0) & SBUF1 (0x99, Page1)
   Write to SFR to Transmit Character (use TB8 also if using 9 bits)
   Read SFR to Receive Character (use RB8 also if using 9 bits)
      NOTE: there are 2 separate buffers here, one is only written to and the other is only read from, but they share the same address.

Enhanced Features for Non-standard Master/Slave Configuration, One Master to Many Slaves used in Multiprocessor Communications

4. UART0 Slave Address – SADDR0 (0xA9, Page 0)
   Set the address of acceptable slave devices

5. UART0 Slave Address Enable – SADEN0 (0xB9, Page 0)
   Enable the slave device addresses

UART0 INITIALIZATION

SCON0: Enable UART0 TX & RX, MODE 01 (8-bit), Check for valid stop bit
SSTA0: Choose desired Divide-by-2 setting, Use TIMER 2 clock for TX & RX (or other clock, but not T1)

Set Up TIMER 2 (or other) & Port 0
RCAP2H & RCAP2L: Set reload value for BAUDRATE
TMR2CF: Set Timer 2 clock input source
TMR2CN: Enable counting, Timer mode, Auto-reload mode
XBR0: Enable UART0 on P0
XBR2: Enable CROSSBAR
P0MDOUT: Set TX & RX for output & input

UART0 INPUT

SCON0: Check RI0
SBUF0: Get 8-bit character if ready

UART0 OUTPUT

SCON0: Check TI0
SBUF0: Load 8-bit character if ready

UART1 INITIALIZATION

SCON1: Enable UART0 TX & RX, MODE 0 (8-bit), Check for valid stop bit, Use clock for TX & RX (TIMER 1)

Set Up TIMER 1 & Port 0
TH1: Set reload value for BAUDRATE
TMOD: Set Timer 1 to Mode 2, SYSCLK clock input source, Enable GATE0
CKCON: Set SYSCLK clock input source/Divide-by
XBR2: Enable CROSSBAR, Enable UART1 on P0
P0MDOUT: Set TX & RX for output & input

UART1 INPUT

SCON1: Check RI1
SBUF1: Get 8-bit character if ready

UART1 OUTPUT

SCON1: Check TI1
SBUF1: Load 8-bit character if ready