C8051F120 MAC (Multiplier Accumulate) Summary

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MAC0CF SFR – setup bits

Since the object is to multiply samples by selected gains and accumulate the result, use the MAC Mode [MAC0CF.0](MAC0MS)

Initially use Integer Mode multiplication for simplicity and let the rounding engine normalize the results [MAC0CF.1](MAC0FM), but you may use Fractional Mode for final program

To start, do not let the Rounding Register saturate, but at some point investigate the effect on performance when this is enabled [MAC0CF.2](MAC0SAT)

To normalize the results, the accumulated sum needs to be shifted right after finishing all the MAC operations [MAC0CF.4](MAC0SD)

MAC0CF SFR – loop operation bits

The accumulator must be cleared before calculating a weighted output value. The other setting may be done once in the initialization program but this operation must be repeated at the beginning of the output calculation loop [MAC0CF.3](MAC0CA)

Each time the Accumulator Shift Control bit is set the accumulator will be shifted by 1 bit. For normalization the data should be shifted 4 or 5 bits to the right after calculating the final result [MAC0CF.5](MAC0SC)

Load the 16-bit ADC input sample x(k) into the A Register [MAC0A or MAC0AH & MAC0AL] Load the 16-bit gain coefficient a_0 into the B Register [MAC0BH & MAC0BL] The low byte of B is loaded last since this transfer initiates the multiply-accumulate operation.

Load the 16-bit previous sample x(k-1) & gain a_1 and repeat for x(k-2), a_2. For advanced filters with feedback, y(k-1), b_1, y(k-2), and b_2 would also be accumulated. Finally add in an appropriate offset (multiplied by 1) to compensate for the fact that the DAC can only go between 0 and +3.0V so +1.5V will be used as the nominal zero output.

Set MAC0SC a few times to normalize the final output (by right shifting the required number of bit positions).

Read the result from appropriate accumulator bytes [MAC0ACC2 & MAC0ACC1 or MAC0ACC1 & MAC0ACC0] (after delay?) and output it to the DAC. Then repeat the loop. (The rounding register [MAC0RND or MAC0RNDH & MAC0RNDL] may also be investigated for output.)