NOTE: Glue logic is not optional! Leaving out the proper chip selection logic when adding memory to the EVB will crash the processor.

0000\textsubscript{16} 8k x 8 bits
1FFF\textsubscript{16} 8 bit data bus, 13 address lines/8k block
2000\textsubscript{16} 8k x 8 bits
3FFF\textsubscript{16}

Top 3 address lines & CSDn used to create chip select signal

Incomplete Address Decoding

Can also ignore A15 & A14, but then physical memory values will appear at multiple addresses! Note: 16k requires 14 address bits.

A15 A14 Not used
A13 Used with CSDn for chip select signal
A12 A0 Connected to chip address lines

Now the 16k block (8k + 8k) will appear 4 times in the 64k range, 0000\textsubscript{16} - 3FF\textsubscript{16} = 4000\textsubscript{16} - 7FF\textsubscript{16} = 8000\textsubscript{16} - BFF\textsubscript{16} = C000\textsubscript{16} - FFF\textsubscript{16} since A15 and A14 are ignored and match any value!
What is the address range of this 4k-memory block?

___ xxxx xxxx xxxx

or

___ 0000 0000 0000  -->  ___ 1111 1111 1111