

C8051F120 12-bit ADC & DAC Summary

Notation: [register.bit] (bit-name)

ADC

SFR PAGE 0 = ADC0_PAGE

Don't need X-bar unless using an external trigger to start conversion (CNVSTR0)

Enable AD0 [ADC0CN.7](AD0EN)

Specify AIN0.0 single-ended or differential channel 0 [AMX0CF.0](AIN01IC)
[AMX0SL.3-.0](AMX0AD3 – AMX0AD0)

Determine input voltage range & set reference voltage (VREFD, J20.7 for external supply)

Set PGA (Programmable Gain Amp) value [ADC0CF.2-.0](AMP0GN2-AMP0GN0) = 000 =>
gain = 1 {available gains: 1, 2, 4, 8, 16, 0.5}

Determine SAR (Successive Approximation Register) clock frequency from SYSCLK
[ADC0CF.7-.3](AD0SC4-AD0SC0) Must be $\leq 2.5\text{MHz}$; see Technical Manual for equation.

Set to continuously track input [ADC0CN.6](AD0TM)

Initiate sampling manually [ADC0CN.3-.2](AD0CM1-AD0CM0)

Use [ADC0CN.4] (AD0BUSY) to determine when sampling is complete

{Don't need Window Compare function}

Choose Right-Justify 12-bit [ADC0CN.0](AD0LJST)

Operating Sequence:

Clear AD0INT

Set AD0BUSY

Wait for AD0INT Flag to go HI

Read data from ADC0H & ADC0L or 16 bits from ADC0

DAC

SFR PAGE 0 = DAC0_PAGE

Select DAC0 Reference Voltage

Enable DAC0 [DAC0CN.7](DAC0EN)

Set multiplier to x1 [DAC0CN.2-.0](DAC0DF2-DAC0DF0) = 000 => gain = 1

Select conversion mode [DAC0CN.4-.3](DAC0MD1-DAC0MD0) = 00

Use manual mode: output updates on a write to DAC0H (**write the HI byte last**)

May also use 16-bit SFR DAC0 to write both bytes together