Micro/Nano-electronics Manufacturing Research at CCNI

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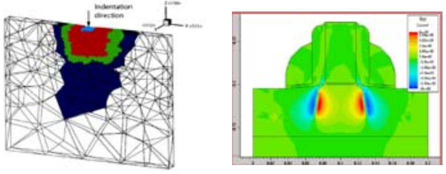
Virtual Nanofabrication

- Nanofabrication requirements constantly changing
  - More aggressive designs in microelectronics and MEMS
  - Advances in biosensors and biomimetics
- Easy to write down a design, difficult to fabricate
  - Must fabricate not one unit, but billions of units (perhaps 500 billion distinct features on a single 300 mm wafer) reliably and economically!
  - Multiple processing steps are chained sequentially, multiplying variability in manufacture.
- Simulation of the multi-step fabrication process
  - Increased optimization of process flows
  - Understanding of manufacturing variability and yield
  - Feedback to designers
    - –Performance simulations on *as fabricated* structures, rather than *as drawn*
    - –Develop increasingly *fab-aware* design rules (DFM/DFY)

Stress-Induced Dislocation Formation in Silicon Devices

Motivation
- At 90 nm and below, devices have come to rely on increased carrier mobility produced by strained silicon.
- How much strain can be built into devices before processing variation and thermo-mechanical loads lead to dislocation nucleation?

Approach
- Concurrent atomistic and continuum simulations, using continuum error estimators to adaptively run molecular dynamics and statics simulations.

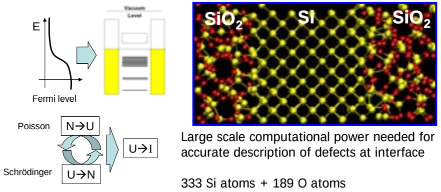


(left) Three-model multiscale simulation of deformation due to nanoindentation. Red/green regions are atomistic simulation, blue is non-linear continuum simulation, and transparent is linear elastic. (right) TSupreme4 simulation of a PFET device, showing *yy* stresses due to material properties mismatch. Combining atomistic simulations with this type of continuum simulation can give insight into how stress concentrations breed device-killing defects.

First-principles Simulations for Device Performance Modeling

Motivation
- Dopant segregation and defect evolution phenomena at silicon interfaces are important for CMOS technology, particularly with high-*k* gate devices.
- Current process modeling are typically based on empirical parameters: needs to be obtained from first principles at nanoscale.

Approach
- First principles methods: Density functional theory (DFT), PBE functional (GGA)
- Focus on various dopants, including B, P, As, F, Ge in Si/SiO2 and SiOxNy interfaces.



Large scale computational power needed for accurate description of defects at interface

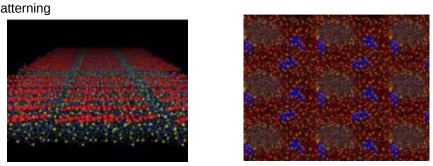
333 Si atoms + 189 O atoms

(left) Schematic of first principles calculation of conduction in a solid. (right) 422 atom structure used to compute the effect of dopants on conduction.

Self-Assembly of Biomolecules on Surfaces

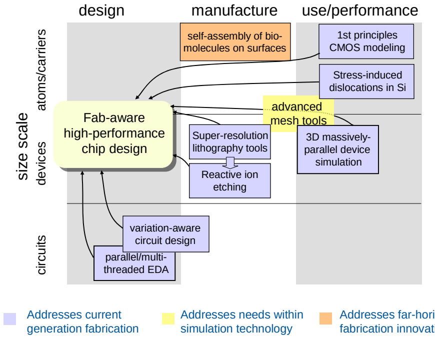
Motivation
- Need to explore options for sub-nanometer patterning, including self-assembly
- Biopolymer self-assembly can generate structures with sub-nm spatial order and molecule-level addressability, but typically occurs in solution
- Extend RPI expertise in biopolymer interactions with soft surfaces (peptide-lipid membrane) to rigid substrates of technological interest
- Basic science research of interest to both IBM and RPI

Open Questions
- what attributes determine the quality and type of ordering when multiple copies are adsorbed on various types of surfaces
- what levels of registration and dimensional control are possible in bio/nano patterning



(left) Protein adsorption on lipid bilayer (right) Toroidal pore formation on a DOPC lipid bilayer by a peptide.

The Micro/Nanoelectronics Simulation Vision



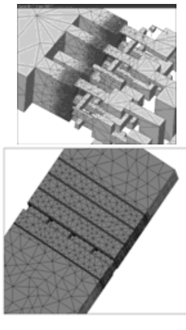
design
manufacture
use/performance
size scale
atoms/carriers
devices
circuits
self-assembly of bio-molecules on surfaces
1st principles CMOS modeling
Stress-induced dislocations in Si
advanced mesh tools
Fab-aware high-performance chip design
Super-resolution lithography tools
Reactive ion etching
3D massively-parallel device simulation
variation-aware circuit design
parallel/multi-threaded EDA

- 🟪 Addresses current generation fabrication
- 🟨 Addresses needs within simulation technology
- 🟧 Addresses far-horizon fabrication innovation

Advanced Meshing Tools for Nanoelectronic Design

Motivation
- Numerical methods within device simulation have changed little within the last 30 years, but devices have become increasingly complex
- Problem sizes and complexities are quickly out stripping the ability to solve.

Approach
- Local refinement, local adaptivity can help carry the computation resources further. “More bang for the buck.
- Leverage existing tools to support FEM-based CCNI projects, such as advanced device modeling.
- Introducing extensions to meet specific needs.

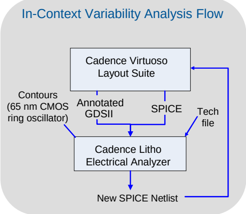


At right is shown a mesh of a single stage of a ring oscillator used in capacitance calculations. ~200k elements, with conductors not shown in mesh for illustration.

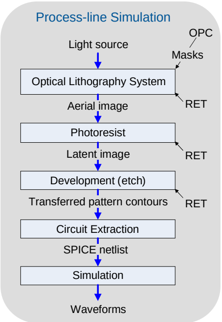
Variation-Aware Circuit Design

Motivation
- There exists a need to characterize the effects of manufacturing variation on final-produce performance and inform the design process.

Approach:
- Create a parallelizable simulation infrastructure for scheduling and running CMOS fabrication process simulation and device modeling tools.
- Leverage commercially demonstrated models and implementations.



In-Context Variability Analysis Flow
Cadence Virtuoso Layout Suite
Contours (65 nm CMOS ring oscillator)
Annotated GDSII
SPICE
Tech file
Cadence Litho Electrical Analyzer
New SPICE Netlist

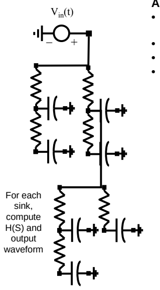


Process-line Simulation
Light source
OPC
Masks
Optical Lithography System
Aerial image
RET
Photoresist
Latent image
RET
Development (etch)
Transferred pattern contours
RET
Circuit Extraction
SPICE netlist
Simulation
Waveforms

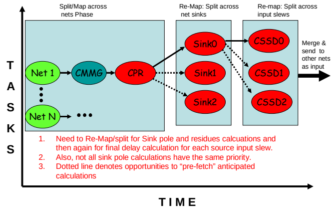
Parallel EDA tools: Using MapReduce to Schedule RICE4

Motivation
- EDA tool data intensity, and data-flow like parallelization.

Approach: MapReduce model
- Targets data-intensive computations
  - Google uses it to compute the PageRank algorithms
- Input data is app-specific and user specified
- Output is a set of <key,value> pairs
- Fault recovery built-in via time-outs on “worker” thread



For each sink, compute H(S) and output waveform

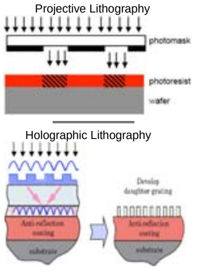


1. Need to Re-Map/split for Sink pole and residues calcuations and then again for final delay calculation for each source input slew.
2. Also, not all sink pole calculations have the same priority.
3. Dotted line denotes opportunities to “pre-fetch” anticipated calculations

Optimization for Super-resolution Nano-lithography

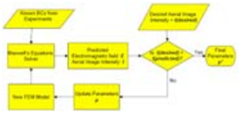
Motivation
- Reducing feature size in semiconductor manufacturing has made the modeling of underlying physics critical.
- In projective lithography simple biases not adequate
- In holographic lithography near-field phenomenon is predominant

Approach
- Solve Maxwell’s equations using a time domain-based, explicit, finite-element code with low dispersion error
- Tight coupling of CAD, meshing and finite element software
- Drive numerical solution with a gradient-based optimization loop to extract grating parameters.

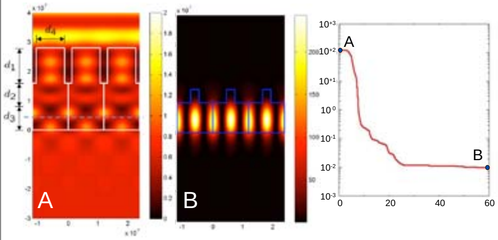


Schematic of two paradigms of lithographic pattern transfer: (top) Projective lithography in which a pattern on a mask is reproduced directly in a photoresist layer. (bottom) Holographic lithography in which a grating produces an interference pattern to produce a secondary mask.

Sample Optimization of Grating



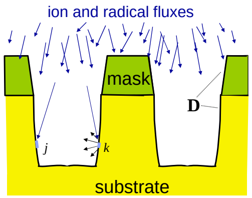
(left) Schematic of approach to grating optimization. (below) Intensity of EM field as a function of position with two different gratings, from initial condition to 60th generation. Note the change in scale, indicating a 4 order of magnitude improvement in the optimization function.



Feature-Scale Modeling of Reactive Ion Etching (RIE)

Motivation
- Transfer of design pattern to wafer is a two-step process: lithography and etch. Of these, etch is the less well-understood step.
- Can we do for etch with OPC has done for lithography?

Approach
- Feature scale models operating on device-sized groups of resist contours, producing cross-sections and 3D representations of etched structures.
- Physically based models, accounting for ballistic transport and chemical mechanisms at vapor-solid interfaces.
- Novel solution techniques to speed computation on industrially relevant structures to practical times.



$$\hat{\eta}_i^{n,t}(j) = \hat{\eta}^{n,1} + \sum_{k\in\mathbf{D}} \hat{q}_{jk}[\hat{\eta}_{i,k}^{n,t} + R_i(\hat{\eta}_k^{n,t}, \hat{\xi}_k, \hat{T}_k)]A_k \quad \text{for } j \in \mathbf{D}$$

Schematic of ballistic transport and reaction model of reactive ion etching on a feature scale. Reactive species are transported to openings in the patterned mask, free from significant homogeneous collisions or reactions on the feature length scale.

Current State of Physically-Based RIE Simulation

Most process codes do not do complex chemistry, using sticking factors or Monte Carlo (or both). Allowing for non-linear chemistry lets you do RIE simulation over a larger range of process conditions

As an example, the simulation on the right uses a generic reactive ion mechanism with diffuse, reactive neutrals and directional ions [1].

Neutral adsorption

$$X(g) + * \rightarrow X^*$$

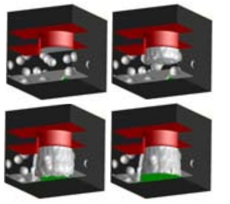
Ion adsorption

$$X^+ + * \rightarrow X^*$$

Ion-assisted etch

$$S + nX^* \rightarrow SX_n + n^*$$

Traditionally this method scales poorly. By necessity, this example is shows a low aspect-ratio, single feature, in a low porosity substrate.



Cut away view of reactive ion etch of an aspect ratio 1.4 via into a dielectric substrate with 7% porosity, and complete selectivity with respect to the underlying etch stop.

[1] Based on J.P. Chang, A.P. Mahorowala, and H.H. Sawin, *J. Vac. Sci. and Technol. A*, **16** (1), p. 217 (1998).

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